

MOTION ADAPTIVE INTERPOLATION WITH MORPHOLOGICAL OPERATION AND 3:2 PULL-DOWNED RECOVERY FOR DEINTERLACING

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Introduction

- ◆ Translate the interlace format of video to progressive device as plasma, projection TV, projector, and computer



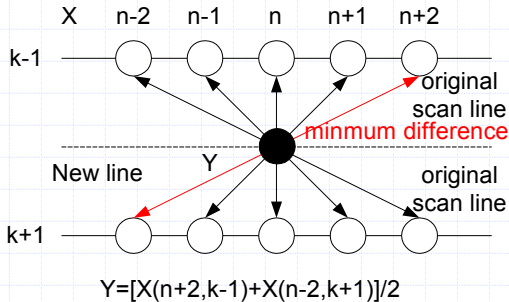
Plasma Display



Previous Work- Intra-Field Interpolation

◆ ELA (Edge Line Average)

- Preserve the edge direction



(a) Bilinear

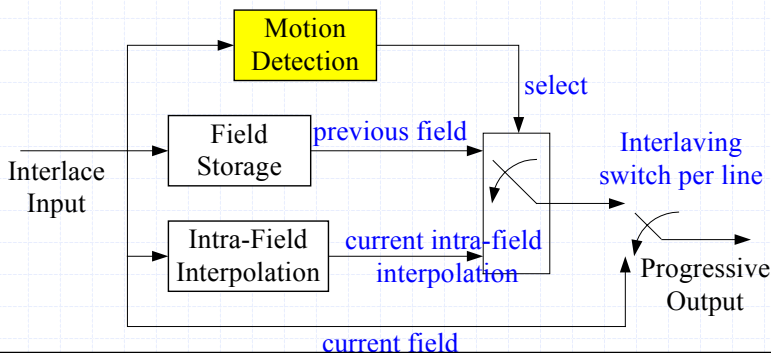


(b) ELA

- ◆ Some defects may be appeared while an object only exists in the same parity field

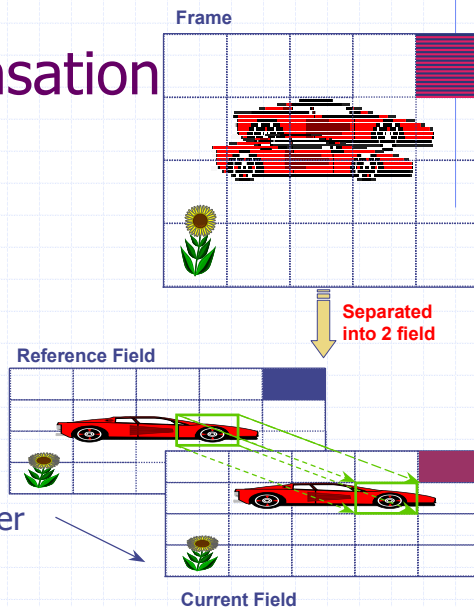
Previous Work- Motion Adaptive Deinterlacing

- ◆ Intra-field interpolation in motion area and inter-field interpolation in static area
 - Needs a reliable motion detection



Previous Work- Motion Compensation

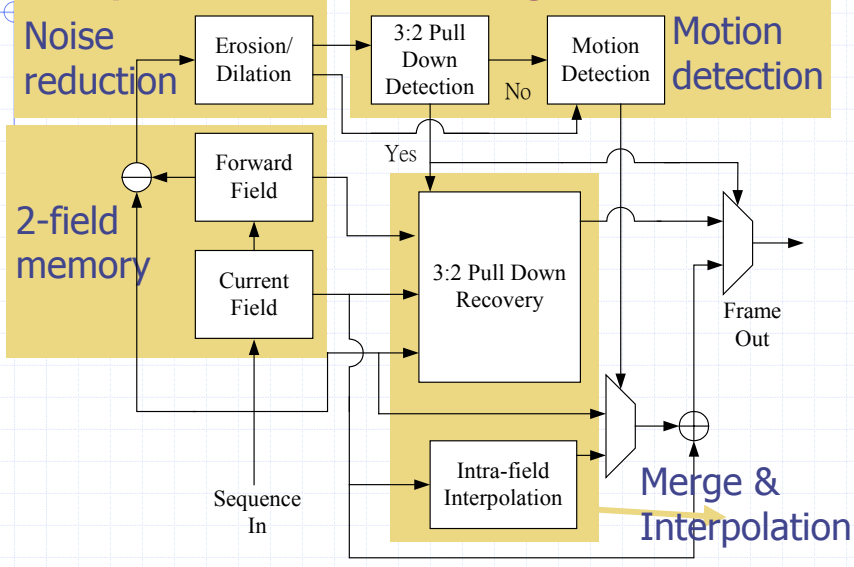
- ◆ Find the matching block in the neighbor field
- ◆ Advantage
 - Can get higher quality
- ◆ Drawback
 - Large computational power
 - Hardware cost is too high



Motivation

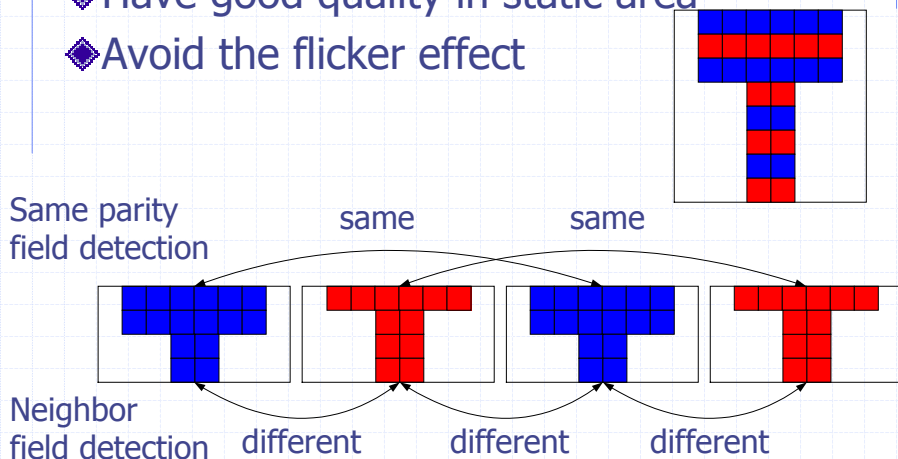
- ◆ Previous Work
 - Intra-field interpolation
 - ◆ Low resolution
 - Motion adaptive deinterlacing
 - ◆ Needs a reliable motion detection
 - Motion compensated deinterlacing
 - ◆ Large computational power and hardware cost
- ◆ Proposed
 - Fast & Cost –efficient method
 - Reliable motion detection

Proposed Block Diagram



Same Parity Field Motion Detection

- ◆ Have good quality in static area
- ◆ Avoid the flicker effect



Morphological Operation

◆ Erosion

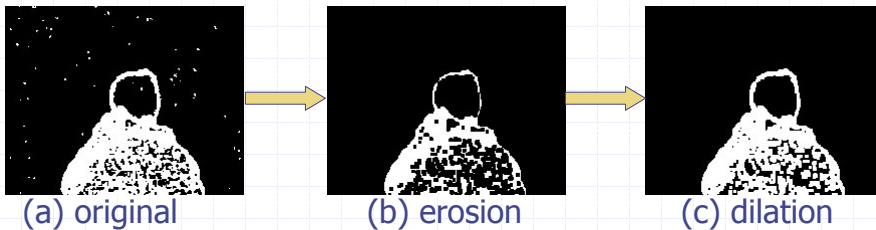
- Noise reduction

$$G(j,k)=\text{MIN}[F(j,k), F(j,k+1), F(j-1,k+1), \dots, F(j+1,k+1)]$$

◆ Dilation

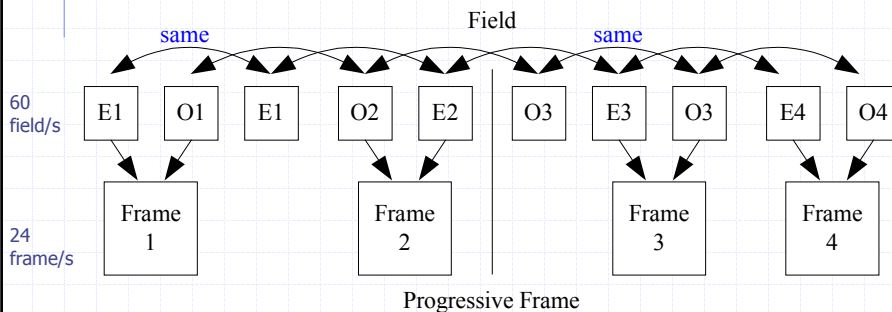
- Expand the motion area

$$D(j,k)=\text{MAX}[G(j,k), G(j,k+1), G(j-1,k+1), \dots, G(j+1,k+1)]$$

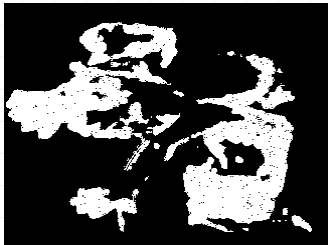


3:2 Pull Down Recovery

- ◆ Same parity detection as motion detection can saving hardware cost



Simulation Results

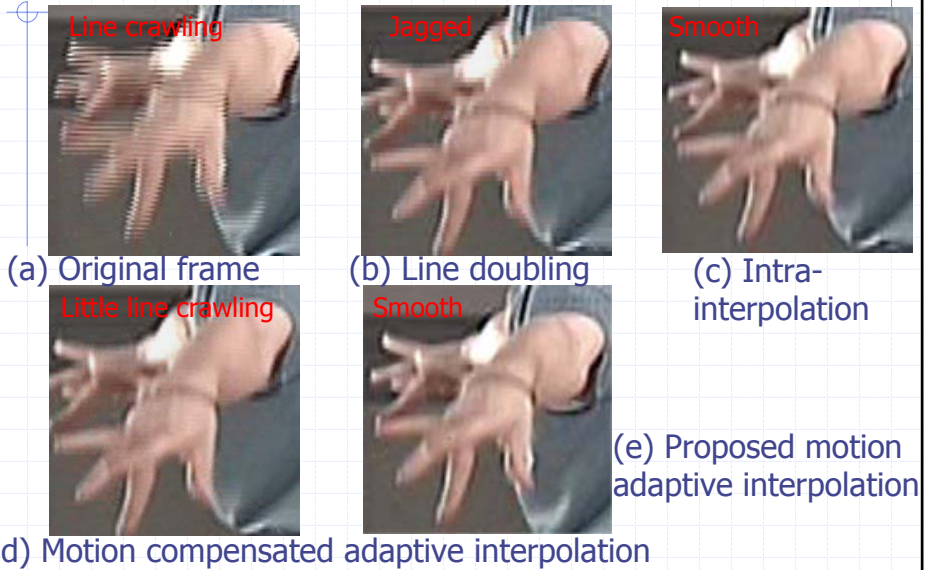


Simulation Results in Static Area

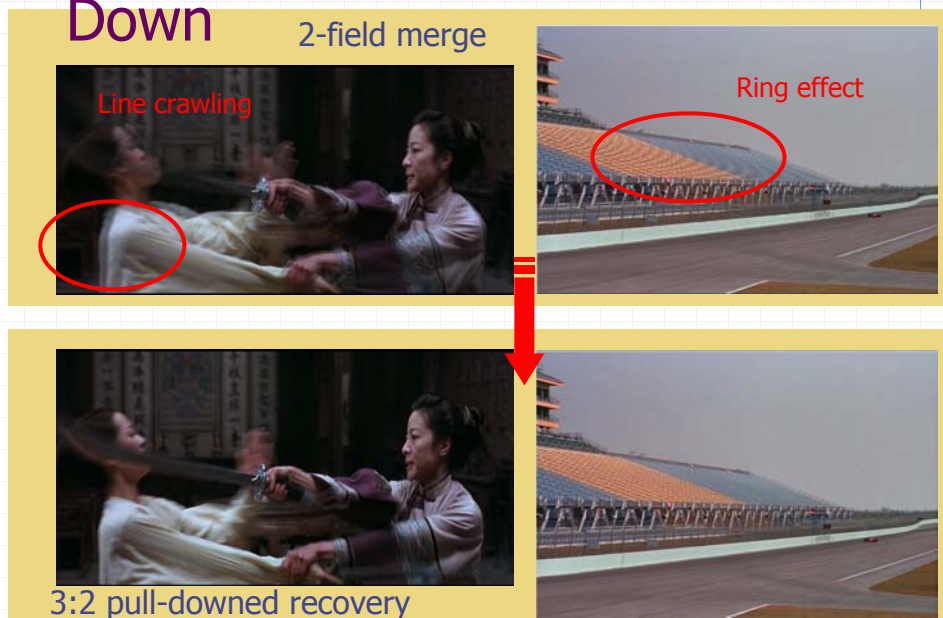


(c) Intra-interpolation (d) proposed motion adaptive interpolation

Simulation Results in Motion Area



Simulation Results for 3:2 Pull Down



Comparison of Hardware Cost

	Complexity	Memory Access Count [pixel]		Memory Usage [byte]	Computational Time [sec/frame]
		Read	Write		
Bilinear	$O(n)$	1	1	1	0.2
ELA	$O(n)$	2	1	10	0.3
M.C.	$O(n^2 \times SR^2)$	226	1	640	10
Proposed	$O(n)$	6	1	9	0.4

n: number of pixels

Athlon K7-700Mhz, 384 Mbytes, Win2000

MC: search range +7~-7, block size 8x8

Conclusions

- ◆ Same parity field check can be adopted in 3:2 pull-down and motion detection circuit for saving hardware-cost.
- ◆ Morphological operation can suppress the visual artifacts and get higher image quality .
- ◆ A fast & efficiently-cost method which is suitable for VLSI design is proposed.